PHASE-LOCKED LOOP

A **phase-locked loop** or **phase lock loop** abbreviated as **PLL** is a control system that generates an output signal whose phase is related to the phase of an input signal. There are several different types; the simplest is an electronic circuit consisting of a variable frequency oscillatorand a phase detector in a feedback loop. The oscillator generates a periodic signal, and the phase detector compares the phase of that signal with the phase of the input periodic signal, adjusting the oscillator to keep the phases matched.

Keeping the input and output phase in lock step also implies keeping the input and output frequencies the same. Consequently, in addition to synchronizing signals, a phase-locked loop can track an input frequency, or it can generate a frequency that is a multiple of the input frequency. These properties are used for computer clock synchronization, demodulation, and frequency synthesis.

Phase-locked loops are widely employed in radio, telecommunications, computers and other electronic applications. They can be used to demodulate a signal, recover a signal from a noisy communication channel, generate a stable frequency at multiples of an input frequency (frequency synthesis), or distribute precisely timed clock pulses in digital logic circuits such as microprocessors. Since a single integrated circuit can provide a complete phase-locked-loop building block, the technique is widely used in modern electronic devices, with output frequencies from a fraction of a hertz up to many gigahertz.

Practical analogies

Automobile race analogy

As an analogy of a PLL, consider an auto race with two cars. One represents the input frequency, the other the PLL's output VCO frequency. Each lap corresponds to a complete cycle. The number of laps per hour (a speed) corresponds to the frequency. The separation of the cars (a distance) corresponds to the phase difference between the two oscillating signals.

During most of the race, each car is on its own and free to pass the other and lap the other. This is analogous to the PLL in an unlocked state.

However, if there is an accident, a yellow caution flag is raised. This means neither of the race cars is permitted to overtake and pass the other car. The two race cars represent the input and output frequency of the PLL in a locked state. Each driver will measure the phase difference (a fraction of the distance around the lap) between himself and the other race car. If the hind driver is too far away, he will increase his speed to close the gap. If he's too close to the other car he will slow down. The result is that both race cars will circle the track in lockstep with a fixed phase difference (or constant distance) between them. Since neither car is allowed to lap the other, the cars make the same number of laps in a given time period. Therefore the frequency of the two signals is the same.

Clock analogy

Phase can be proportional to time, so a phase difference can be a time difference. Clocks are, with varying degrees of accuracy, phase-locked (time-locked) to a master clock.

Left on its own, each clock will mark time at slightly different rates. A wall clock, for example, might be fast by a few seconds per hour compared to the reference clock at NIST. Over time, that time difference would become substantial.

To keep the wall clock in sync with the reference clock, each week the owner compares the time on his wall clock to a more accurate clock (a phase comparison), and he resets his clock. Left alone, the wall clock will continue to diverge from the reference clock at the same few seconds per hour rate.

Some clocks have a timing adjustment (a fast-slow control). When the owner compared his wall clock's time to the reference time, he noticed that his clock was too fast. Consequently, he could turn the timing adjust a small amount to make the clock run a little slower (frequency). If things work out right, his clock will be more accurate than before. Over a series of weekly adjustments, the wall clock's notion of a second would agree with the reference time (locked both in frequency and phase within the wall clock's stability).

An early electromechanical version of a phase-locked loop was used in 1921 in the Shortt-Synchronome clock.

History

Spontaneous synchronization of weakly coupled pendulum clocks was noted by the Dutch physicist Christiaan Huygens as early as 1673. Around the turn of the 19th century, Lord Rayleigh observed synchronization of weakly coupled organ pipes and tuning forks. In 1919, W. H. Eccles and J. H. Vincent found that two electronic oscillators that had been tuned to oscillate at slightly different frequencies but that were coupled to a resonant circuit would soon oscillate at the same frequency. Automatic synchronization of electronic oscillators was described in 1923 by Edward Victor Appleton.

Earliest research towards what was later named the phase-locked loop goes back to 1932, when British researchers developed an alternative to Edwin Armstrong's superheterodyne receiver, the Homodyne or direct-conversion receiver. In the homodyne or synchrodyne system, a local oscillator was tuned to the desired input frequency and multiplied with the input signal. The resulting output signal included the original modulation information. The intent was to develop an alternative receiver circuit that required fewer tuned circuits than the superheterodyne receiver. Since the local oscillator would rapidly drift in frequency, an automatic correction signal was applied to the oscillator, maintaining it in the same phase and frequency of the desired signal. The technique was described in 1932, in a paper by Henri de Bellescize, in the French journal *L'Onde Électrique*.

In analog television receivers since at least the late 1930s, phase-locked-loop horizontal and vertical sweep circuits are locked to synchronization pulses in the broadcast signal.

When Signetics introduced a line of monolithic integrated circuits like the NE565 that were complete phase-locked loop systems on a chip in 1969, applications for the technique multiplied. A few years later RCA introduced the "CD4046" CMOS Micropower Phase-Locked Loop, which became a popular integrated circuit.

Structure and function

Phase-locked loop mechanisms may be implemented as either analog or digital circuits. Both implementations use the same basic structure. Both analog and digital PLL circuits include four basic elements:

- Phase detector,

- Low-pass filter,
- Variable-frequency oscillator, and
- feedbackpath (which may include a frequency divider).

Variations

There are several variations of PLLs. Some terms that are used are analog phase-locked loop (APLL) also referred to as a linear phase-locked loop (LPLL), digital phase-locked loop (DPLL), all digital phase-locked loop (ADPLL), and software phase-locked loop (SPLL).

Analog or linear PLL (APLL)

Phase detector is an analog multiplier. Loop filter is active or passive. Uses a voltage-controlled oscillator (VCO).

Digital PLL (DPLL)

An analog PLL with a digital phase detector (such as XOR, edge-trigger JK, phase frequency detector). May have digital divider in the loop.

All digital PLL (ADPLL)

Phase detector, filter and oscillator are digital. Uses a numerically controlled oscillator (NCO).

Software PLL (SPLL)

Functional blocks are implemented by software rather than specialized hardware.

Neuronal PLL (NPLL)

Phase detector, filter and oscillator are neurons or small neuronal pools. Uses a rate controlled oscillator (RCO). Used for tracking and decoding low frequency modulations (< 1 kHz), such as those occurring during mammalian-like active sensing.

Performance parameters[edit]

Main article: Phase-locked loop ranges

- Type and order
- Hold-in range
- Pull-in range (capture range, acquisition range)
- Lock-in range
- Loop bandwidth: Defining the speed of the control loop.
- Transient response: Like overshoot and settling time to a certain accuracy (like 50ppm).
- Steady-state errors: Like remaining phase or timing error.
- Output spectrum purity: Like sidebands generated from a certain VCO tuning voltage ripple.
- Phase-noise: Defined by noise energy in a certain frequency band (like 10 kHz offset from carrier). Highly dependent on VCO phase-noise, PLL bandwidth, etc.
- General parameters: Such as power consumption, supply voltage range, output amplitude, etc.